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Wavelength-Division Multiplex Small Form Factor Pluggable (PXFP-WDM) Optical Transmitter Module Interface Specification

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Table of Contents

List of Figures

List of Tables

1. Introduction

1.1. Executive Summary

Many service provider networks are fiber constrained. The cost of fiber construction is prohibitive in most applications and many service provider systems have link distances that significantly exceed 20 km. The use of a PON Extender architecture utilizing WDM optics enables multiple 10G PON links to be deployed on different wavelengths over a single fiber at distances much greater than 20 km.

WDM pluggable optics compatible with PON OLT line cards enable a multi-wavelength link between the OLT platform and a PON Repeater. This standard defines these optics for use in PON OLTs.

1.2. Scope

A PON Extender architecture utilizing WDM optics enables 10GEPON to be deployed over limited fibers and distances over 20 km. Figure 1 shows a typical system use case for a PON Extender architecture.

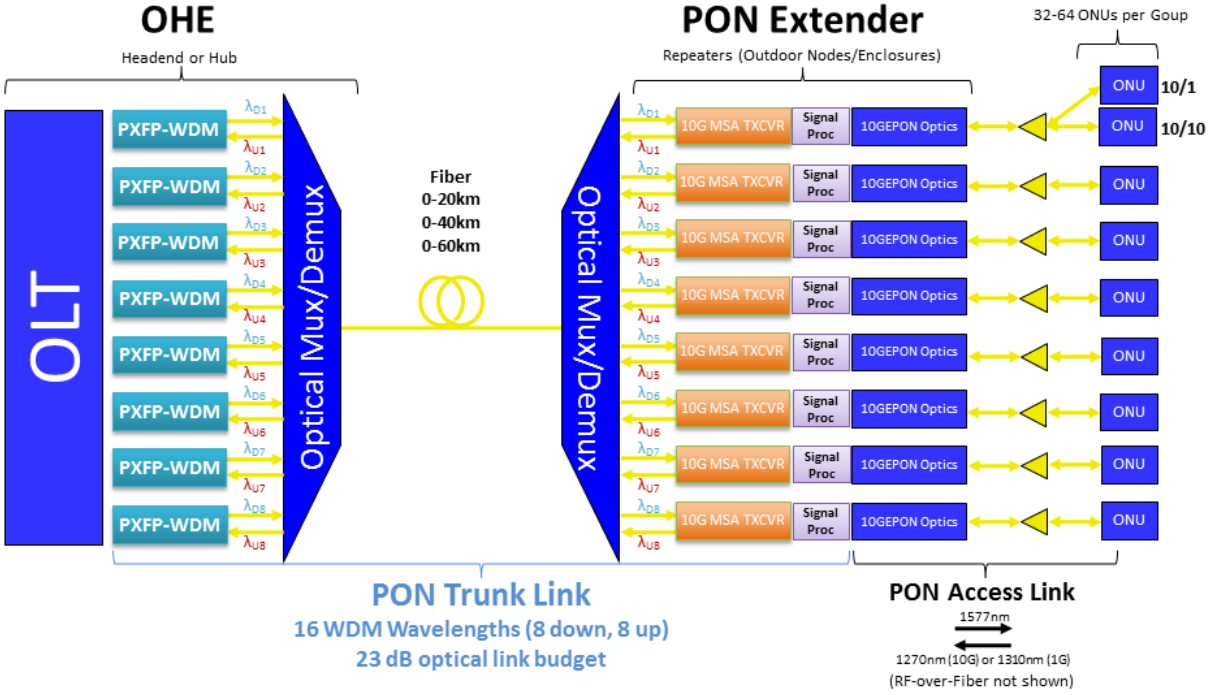

Figure 1 – Typical System Use Case for PON Extender

This specification focuses on the communications, electrical, optical, and mechanical interfaces for the Wavelength-Division Multiplex Small Form Factor Pluggable transceiver module (PXFP-WDM). PXFP-WDM is a pluggable optical transceiver module. The basic requirements are plugging into existing XFP ports in the OLT and having CWDM or DWDM 2-fiber optics (1 port for transmit and 1 port for receive). The downstream data rate is 10 Gb/s in continuous mode. The upstream data rate is a mix of 10 Gb/s and 1.25 Gb/s in continuous mode to handle co-existence of 10/10 and 10/1 ONU's in the same PON group.

Note: The PON Extender converts the upstream data from the PON Access Link from burst-mode to continuous mode.

1.2.1. PON Extender Access Using Channel Add-Drop Mux

The point-to-point architecture in Figure 1can be extended to a cascaded access network as shown in Figure 2, where PON extenders of single-channel or dual-channel OLTs are connected on the respective wavelength by using the WDM Channel Add-Drop Mux (CH ADM). Note that the CH ADM does not have to be incorporated into the PON Extender as depicted here, but could be external. This architecture offers the flexibility to reach more clusters of residential areas. In each area only the necessary hardware is installed and can be added on a pay-as-you-grow basis.

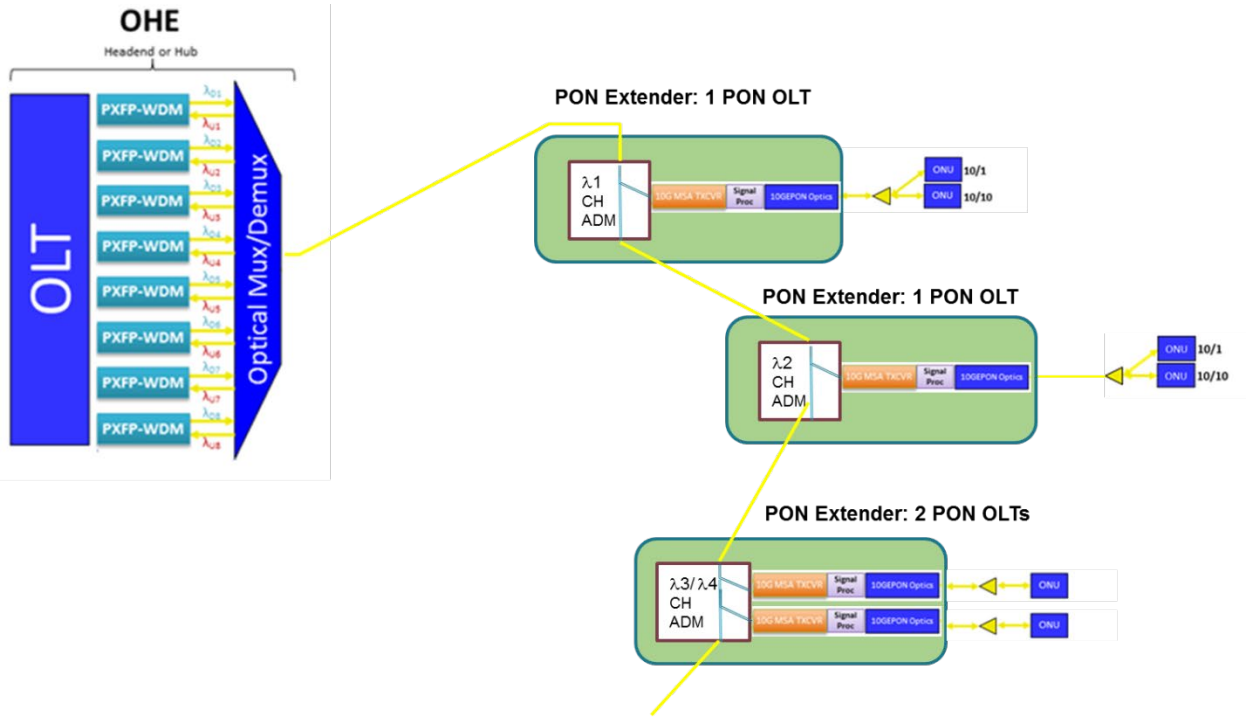

Figure 2 - PON Extender Access Using Channel Add-Drop Mux

1.3. Benefits

The benefits of a WDM-capable XFP pluggable optical interface include:

- Distance gains: XFP PON optics only support distances of up to 20 km. WDM optics support distances of up to 60 km. Coupling this capability with PON Extender devices, the service provider's optical plant can be extended well beyond what can be supported today.
- Fiber savings: XFP PON optics are fixed wavelength – a digital PON link cannot coexist on a single fiber with other digital PON links. Wave-division multiplexing allows multiple PON links to be placed on the same fiber at different wavelengths, allowing the same fiber to deliver multiple PON links.
- Commodity optics: WDM-capable optics for PON OLTs were previously only available as custom optics, increasing price and decreasing availability. This standard enables the manufacture of interoperable pluggable interfaces, reducing costs and compatibility issues.

1.4. Intended Audience

This specification is intended for optics vendors and provides detailed requirements to allow the manufacture of interoperable, standardized pluggable optical interfaces for this use case.

2. Normative References

The following documents contain provisions, which, through reference in this text, constitute provisions of this document. At the time of Subcommittee approval, the editions indicated were valid. All documents are subject to revision; and while parties to any agreement based on this document are encouraged to investigate the possibility of applying the most recent editions of the documents listed below, they are reminded that newer editions of those documents might not be compatible with the referenced version.

2.1. SCTE References

- No normative references are applicable.

2.2. Standards from Other Organizations

Reference	Description
[DWDM]	ITU G.698.1, November, 2009, Series G: Transmission Systems and Media, Digital Systems and Networks, Transmission media and optical systems characteristics – Characteristics of optical systems, Multichannel DWDM applications with single-channel optical interfaces.
[DWDM-GRID]	ITU G.694.1, February, 2012, Series G: Transmission Systems and Media, Digital Systems and Networks, Transmission media and optical systems characteristics – Characteristics of optical systems, Spectral Grids for WDM applications: DWDM frequency grid.
[FINISH]	IEC 61300-3-35, ed. 1.0, November 20, 2009, Fibre optic interconnecting devices and passive components - Basic test and measurement procedures - Part 3-35: Examinations and measurements - Fibre optic connector endface visual and automated inspection, IEC Sub-committee 86B
[IEC 61754-20]	IEC 61754-20:2012 Fibre optic interconnecting devices and passive components - Fibre optic connector interfaces - Part 20: Type LC connector family
[IEC 61755-3-1]	IEC 61755-3-1:2006, ed. 1.0, July 1, 2006, Fibre optic connector optical interfaces – Part 3-1: Optical interface, 2,5 mm and 1,25 mm diameter cylindrical full zirconia PC ferrule, single mode fibre. IEC Sub-committee 86B
[XFP MSA]	INF-8077i, Revision 4.5, August 31, 2005, 10 Gigabit Small Form Factor Pluggable Module, SFF Committee
[SFF-8477]	SFF-8477, Revision 1.4, December 4, 2009, Tunable XFP for ITU Frequency Grid Applications, SFF Committee

2.3. Published Materials

Reference	Description
[UM10204]	UM10204, Version 4.0, February 13 2012, The I2C-Bus specification and user manual, NXP Semiconductors

3. Informative References

The following documents might provide valuable information to the reader but are not required when complying with this document.

3.1. SCTE References

- No informative references are applicable.

3.2. Standards from Other Organizations

Reference	Description
[IEEE 802.3]	IEEE Standard for Information Technology-Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CMSA/CD) Access Method and Physical Layer Specifications, IEEE 802.3-2012

3.3. Published Materials

- No informative references are applicable.

4. Compliance Notation

shall	This word or the adjective "***required***" means that the item is an absolute requirement of this document.
shall not	This phrase means that the item is an absolute prohibition of this document.
forbidden	This word means the value specified shall never be used.
should	This word or the adjective "*recommended*" means that there may exist valid reasons in particular circumstances to ignore this item, but the full implications should be understood and the case carefully weighted before choosing a different course.
should not	This phrase means that there may exist valid reasons in particular circumstances when the listed behavior is acceptable or even useful, but the full implications should be understood and the case carefully weighed before implementing any behavior described with this label.
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deprecated	Use is permissible for legacy purposes only. Deprecated features may be removed from future versions of this document. Implementations should avoid use of deprecated features.

5. Abbreviations

Abbreviation	Term
APD	avalanche photodiode
BOL	beginning of life
CDR	clock data recovery
DWDM	Dense Wavelength Division Multiplexing

Abbreviation	Term
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
EOL	end of life
I^2C	two-wire communications interface
LOS	loss of signal
MSA	multi-source agreement
OHE	optical headend
OLT	optical line terminal
ONU	optical network unit
PCB	printed circuit board
PON	Passive Optical Network
Rx	receive
SCL	serial clock
SDA	serial data
SERDES	serializer/deserializer
SFP	small form factor pluggable module
Tx	transmit
UPC	Ultra Physical Contact connector end-face
WDM	Wavelength Division Multiplexing
XFP	10 gigabit small form factor pluggable module
PXFP-WDM	A WDM-capable transceiver module with an XFP form factor

6. Management Interface

2-Wire Communications (I²C) for the PXFP-WDM module are based upon [XFP MSA]. I²C is an implementation of the NXP (formerly Philips) I²C [UM10204] specification with mapped memory address locations (also known as "well-known addresses") for diagnostics and operations. The SFF Committee specifies the I²C common memory mapping in [XFP MSA] and [SFF-8477] for SFP and XFP, as well as additional physical layer requirements. This specification uses the same well-known memory map locations (addresses) for functions that are the same or substantially similar. Some memory map fields from [XFP MSA] and [SFF-8477] are re-allocated or not used; in addition, some memory map fields have been added.

The PXFP-WDM module ***shall*** implement the I^2C requirements specified in [XFP MSA], except where specified differently in the following sections.

6.1. Summary of 2-Wire Communications Requirements

In [XFP MSA] 2-wire communication requirements are spread across several sections, including Section 4.2 and Table 26, Section 2.6 and Table 3. The following bullets summarize the requirements in [XFP MSA]; refer to [XFP MSA] for complete details.

- I²C communications *may* not be available for up to 300 ms after power up or reset
- The I^2C interface bus of the PXFP-WDM module is not a shared one, in contrast to that of the XFP module, as it does not have a Mod_DeSel pin.
- There must be at least 20 µs between the STOP signal and the next START signal for a particular module.
- The clock rate can be as high as 400 kHz (I²C fast mode).

- Up to two START signals per command are allowed (the second START is also known as a RESTART signal).
- Only one STOP signal is allowed per command.
- Multiple master systems are not supported.
- Host boards ***shall*** accommodate PXFP-WDM modules which hold the SCL line *low* (clock stretching) for up to a maximum of 500 µs during an I²C read or write operation.
- After a write from the host to the module, the module *may* not respond to further I²C commands for up to 40 ms (typically this would be for writing non-volatile values). The phrase "not respond" means that the device address given immediately after the START signal from the host is not acknowledged by the module.
- I²C packet error checking protocol is optional as defined in the [XFP MSA].

6.2. Theory of Operation

Using Chapter 5: Management Interface of [XFP MSA] as reference, the following sections define the operation of the PXFP-WDM module I²C interface that is used for serial ID, digital diagnostics and other control/monitoring functions.

6.2.1. PXFP-WDM Module Boot Up Sequence

When a PXFP-WDM module is plugged in, the host needs to perform a number of initialization steps in a particular order with a particular timing. Some of these involve the PXFP-WDM module pins and some involve I²C communications. As most of these are documented in the [XFP MSA] or are implied by stated dependencies, a reference to the location(s) in that document will accompany each step in the following sequence descriptions.

Before the boot up sequence can be discussed, communications and host requirements need to be understood.

6.2.1.1. I²C Communications Requirements

Once I²C is operational, the host ***shall*** adhere to the timing requirements defined in Section 4.2, Table 26 of [XFP MSA].

Write operations *may* cause the PXFP-WDM module to not respond to further I²C signals or messages for up to 40 ms (t_{WR} in Section 4.3, Table 27, and Section 4.5.7 of [XFP MSA]). The specification does not restrict this to EEPROM writes. This applies for writes from one to four bytes (the limit for a write is four bytes).

The PXFP-WDM module *may* perform a clock stretch of up to 500 µs during read or write operations (T_clock_hold, [XFP MSA] Section 4.3, Table 27). This is distinct from unresponsiveness after a write operation (t_{WR}).

6.2.1.2. Pin State Prior to PXFP-WDM Module Boot Up

Before a PXFP-WDM module can begin boot up, the host ***shall*** meet the following pin requirements.

The voltages listed for pins 6 (VCC5), 8 (VCC3_Tx), and 9 (VCC3_Rx) in Table 4 ***shall*** be available.

6.2.1.3. Initial PXFP-WDM Module Boot Sequence

Once the PXFP-WDM module is inserted, it goes through its initialization sequence, as shown in the following flow chart.

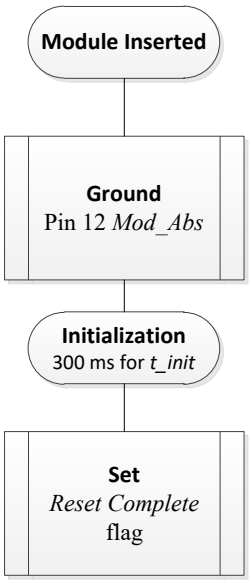

Figure 3 – PXFP-WDM Module Boot Sequence

This series of actions is described here.

1. The PXFP-WDM module ***shall*** indicate its presence to the host by grounding pin 12 (Mod_Abs) upon insertion.
2. After 300 ms, PXFP-WDM module initialization (aka *Reset Complete*, described in Table 39 of [XFP MSA]) ***shall*** be finished (t_init, [XFP MSA] Section 2.6, Table 3).
3. The PXFP-WDM module ***shall*** set the *Reset Complete* flag ([XFP MSA] Section 2.4.7.3, Table 39). *Reset Complete* can be detected by the host by reading the *Reset Complete* flag to determine if it is set.

Note that until the boot sequence is complete, pin signals might not be valid, as detailed in Section 2.4.7.3 of [XFP MSA].

The *Reset Complete* flag does not imply that registers are valid; the module sets the *Data_Not_Ready* flag (from Table 42 in [XFP MSA]) to *low* to indicate that register contents are valid and can be read.

6.2.2. Host Initialization of the PXFP-WDM Module

After completion of the PXFP-WDM module boot sequence, the host ***shall*** initialize the module, including interrupt masks, as detailed in the following flow chart.

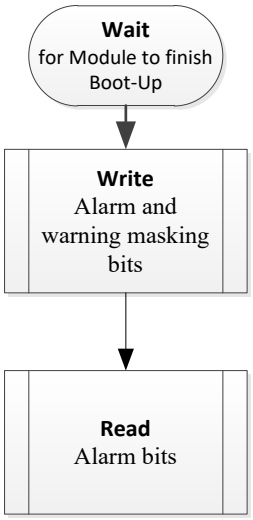

Figure 4 – Host PXFP-WDM Module Initialization

This series of actions is described here.

The host can set alarm and warning masks for any events of interest. These can be found in Table 40 in Section 5.11.1 of [XFP MSA] with the exception of those alarms and warnings listed in section 6.4.2, Lower Memory Map (Common Table). By default none of these is masked. In particular, the *Reset Complete* status bit is not masked. At a minimum, the host *should* set the masking bits for:

- Receiver values (RX Power, RX_NR Status, RX_LOS)
- APD Supply (which is not supported)
- Wavelength Unlocked

The host can clear any existing latched alarms by reading those alarm bits (the alarm bits are listed in Table 39 in Section 5.11.1 of [XFP MSA]). As these flags are latched, their initial presence does not necessarily indicate a continuing fault. For example, the presence of the *Reset Complete* flag upon insertion of the module is not a fault. During initialization the PXFP-WDM module *may* not have set the TX Bias and TX Power before testing for errors. Among those that can be reasonably expected are:

- TX_NR Status
- Receiver values as listed above
- Reset Complete
- Wavelength Unlocked
- TX Bias Low
- TX Power Low

6.2.3. Interrupt Conditions from the PXFP-WDM Module

The following section is based on Section 5.11 of [XFP MSA]; modifications have been made for this specification.

In order to alert the host system to any condition outside of normal operating conditions, the PXFP-WDM module implements an Interrupt bit in byte 110; when the Interrupt bit is set, the host checks the alarm and warning flags to determine the condition. The host is required to periodically check the state of the Interrupt bit.

The PXFP-WDM module ***shall*** set the Interrupt bit and latch the appropriate alarm flags when an alarm condition occurs. The following types of alarm flags are provided:

- Alarm and warning flags as described in section 5.6, Basic Monitoring Functions of [XFP MSA]. These correspond to monitored quantities going outside factory programmed threshold values.
- Flags corresponding to basic PXFP-WDM module status conditions including:
    - TX_NR: Any condition leading to invalid data on the TX path
    - TX_Fault: Laser fault condition
    - MOD_NR: Module Not Ready
    - Reset Complete: Indicates completion of the PXFP-WDM Module Reset
- Flags corresponding to optional extended capabilities including TEC Fault.

This specification uses byte 85, bit 0 for a vendor-specific alarm.

Existence of any of these conditions ***shall*** lead to a latched flag. These flags are located in bytes 80 – 87 and are detailed in Table 39 of [XFP MSA]. The presence of any 1 value in bytes 80 – 87 without a corresponding mask bit set to 1 will assert the Interrupt bit in byte 110.The host *may* query the latched flag bits in bytes 80 – 87. The PXFP-WDM module ***shall*** clear the latched flags upon the read of the corresponding latched flag bit.

Masking bits ***shall*** be volatile and startup with all unmasked (masking bits 0).

The mask bits can be used to prevent continued interruption from ongoing conditions. This specification uses byte 93, bit 0 for the vendor-specific alarm mask.

6.3. PXFP-WDM Module Memory Map

The structure of the PXFP-WDM module memory map is shown in Figure 5. The PXFP-WDM module ***shall*** implement the memory map specified in section 5 of [XFP MSA] and section 4 of [SFF-8477], with the exceptions specified here.

The normal 256 byte I²C address is divided into lower and upper blocks of 128 bytes. The lower block of 128 bytes is always directly available and is intended to be used for diagnostic and control functions that are accessed often. This is the common table; it is accessed if the I²C address is less than 128 without regard to the selected table.

Multiple blocks of memory are available in the upper 128 bytes of the address space. These are individually addressed via a table select byte located in the lower address space (at offset 127). The upper address tables are intended to contain information that is accessed less frequently, such as serial ID, user writable EEPROM, etc. The password must be entered before any upper memory can be accessed. The password entry stays in effect until the module is power cycled.

Figure 5 summarizes the memory layout. The major difference from [XFP MSA] is that some fields are not supported or used differently, as detailed in section 6.4.2.

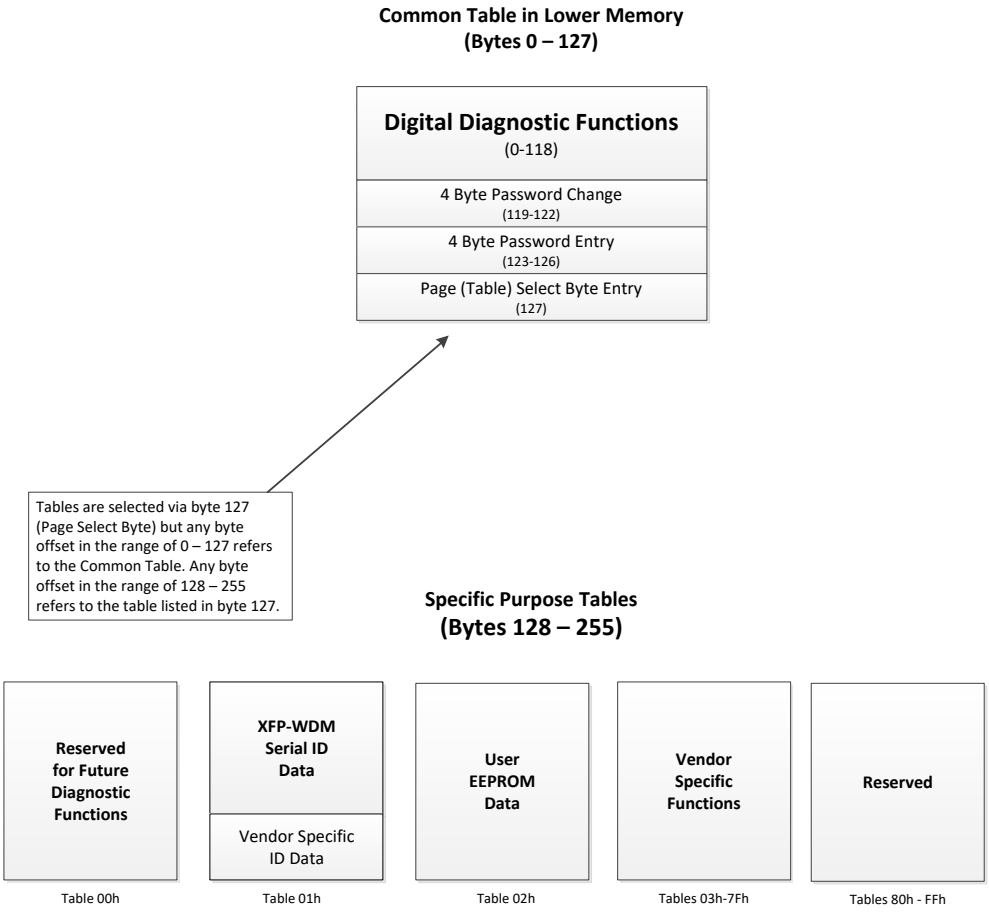

Figure 5 – PXFP-WDM Module Memory Layout

6.4. Specific Memory Maps

6.4.1. Volatile and Non-Volatile Field Characteristics

6.4.1.1. Non-Volatile Field Resilience

The PXFP-WDM module ***shall*** meet the [XFP MSA] specification requirement for EEPROM write cycles (at least 50,000 write cycles). If a host were to write to such a field once per minute, then the EEPROM would expire in roughly 35 days. Writing once per hour gives a lifetime of about 5.7 years.

6.4.1.2. Access Rate for Volatile and Read-Only Fields

While there is no maximum rate for these fields, there is an I²C limitation. Therefore, the host *should not* expect "tight loop" level of control.

6.4.2. Lower Memory Map (Common Table)

The lower 128 bytes of the I²C serial bus address space is used to access a variety of measurements and diagnostic functions, and to implement a set of control functions. The contents of the lower memory map ***shall*** conform to the [XFP MSA] I²C specification unless specified otherwise below.

- The following values are not used by the PXFP-WDM module. They are not repurposed. The PXFP-WDM module ***shall*** set all of these values to 0. The host ***shall*** ignore all of these bits. These include:
    - Line-side Loopback Control
    - XFI Loopback Control
    - Acceptable BER for FEC system
    - Actual BER for FEC system
    - FEC Amplitude Adj
    - FEC Phase Adj
    - Data Rate Control
    - Signal Conditioner Control
    - Vcc2 High Alarm
    - Vcc2 Low Alarm
    - Vee5 High Alarm
    - Vee5 Low Alarm

- The value of the Identifier field ***shall*** be 0x80 (PXFP-WDM) rather than 06h (XFP).

- In bytes 10 – 17, 80, 82, 88, and 90, the Reserved values ***shall*** correspond to VCC3.

6.4.3. General Control and Status Bits

The control and status bits supporting the WDM-XFP module mirror those described in Section 5.11.1 and Table 42 of [XFP MSA] with the exceptions detailed in Table 1.

Table 1 – General Control/Status Bits

Byte	Bit	Name	Description
110	4	Reserved	In the XFP MSA, this bit mirrors the P_DOWN pin state; this pin is not implemented in the WDM-XFP.

6.4.4. Upper Memory Maps

The upper address space tables are used for less frequently accessed functions such as serial ID, user writable EEPROM, reserved EEPROM and diagnostics and control spaces for future standards definition, as well as Manufacturing ID and security code. These are allocated as follows:

- Table 00h: Reserved for future diagnostic and control functions
- Table 01h: PXFP-WDM Serial ID Data and Vendor Specific ID Data
- Table 02h: User writable EEPROM (with optional Common Language Equipment Identification (CLEI))

6.4.4.1. PXFP-WDM Serial ID Data and Vendor Specific ID Data: Table 01h

The serial ID memory map located in Table 01h in the upper address space is used for read-only identification information, except for the last 32 bytes which are Vendor EEPROM. The Identifier field at byte 128 is a duplicate of the Identifier field at byte 0 and *should* be set to the same value.

The contents of the vast majority of the fields ***shall*** be as indicated in [XFP MSA] with the following exceptions:

- *Identifier* is set to the same value as the Identifier field at byte 0
    - In the *Auxiliary Input Type* (byte 222), nibble 0111b is now a Reserved field. All other nibbles are as defined in Table 59 of [XFP MSA].

Table 2 – Auxiliary Input Types

Value	Description of physical device
0111b	Reserved

6.4.4.2. User Writable EEPROM Data: Table 02h

Table 02h is provided as user EEPROM, as explained in [XFP MSA]. The host system can read and write this memory for any purpose. If bit 3 of Table 01h, byte 129 is set, however, the first 10 bytes of Table 02h [128 – 137] will be used to store the CLEI code for the module. This does not imply that these 10 bytes are read-only.

6.4.4.3. Byte 252 – OLT Type

Byte 252 is used to identify the type of OLT in which the WDM-XFP module was installed. The values are as listed in Table 3.

Table 3 – OLT Types

Bit	Description
0	Type 1 (Tx 10G / Rx 1G)
1	Type 2 (Tx 10G / Rx 10G)
2	Type 3 (Tx 10G & 1G / Rx 1G)
3	Type 4 (Tx10G & 1G / Rx 1G & 10G)
4	DWDM OLT (Tx 10G / Rx 10G & 1G)
5	Reserved
6	Type 2-1 (Tx 10G / Rx 10G & 1G) for extender
7	1G OLT (Tx 1G / Rx 1G)

7. Electrical Interface

7.1. Introduction

The electrical interface of the PXFP-WDM module is the same as defined in [XFP MSA] with a few exceptions, as detailed here.

Note: The PXFP-WDM module is designed for use in PON OLT devices and is NOT MSA standard compliant. Plugging the PXFP-WDM module into an MSA standard receptacle may result in damage to the host and/or module.

7.2. Pinout

The PXFP-WDM module and host ***shall*** conform to the electrical pin definitions specified in Table 4 and the subsections within Section 7.2.1.

Table 4 – PXFP-WDM Module Electrical Pin Definition

Pin	Logic	Symbol	Name/Description	Plug Sequence	Note
1		GND	Module ground	1	1
2		NC	Not connected	3	
3		NC	Not connected	3	
4		GND	Module ground	1	1
5	LVTTL-I	TX_DIS	Transmitter disable; Turns off transmitter laser output	3	3
6		VCC5	+5 V power supply	2	
7		GND	Module ground	1	1
8		VCC3_Tx	+3.3 V power supply for transmitter	2	
9		VCC3_Rx	+3.3 V power supply for receiver	2	
10	LVTTL-I/O	SCL	I^2C serial interface clock	3	2
11	LVTTL-I/O	SDA	I^2C serial interface data line	3	2
12	LVTTL-O	MOD_ABS	Indicates module is not present. Grounded in the module.	3	2
13		NC	Not connected	3	
14	LVTTL-O	Rx_LOS	Receiver loss of signal indication output	3	2
15		GND	Module ground	1	1
16		GND	Module ground	1	1
17	LVCML-O	Rx_10G_N	Receive inverted 10.3125 Gb/s data output. DC coupled inside the module.	3	
18	LVCML-O	Rx_10G_P	Receive non-inverted 10.3125 Gb/s data output. DC coupled inside the module.	3	
19		GND	Module ground	1	1
20	LVPECL-O	Rx_1G_N	Receive inverted 1. 25 Gb/s data output. DC coupled inside the module.	3	4
21	LVPECL-O	Rx_1G_P	Receive non-inverted 1.25 Gb/s data output. DC coupled inside the module.	3	4
22		NC	Not connected	2	6
23		NC	Not connected	3	6
24		NC	Not connected	3	6
25		NC	Not connected	3	6
26		NC	Not connected	3	6
27		GND	Module ground	1	1
28	LVCML-I	TX_10G_N	Transmit inverted 10.3125 Gb/s data output. AC coupled inside the module.	3	5
29	LVCML-I	TX_10G_P	Transmit non-inverted 10.3125 Gb/s data output. AC coupled inside the module.	3	5
30		GND	Module ground	1	1

1. Module ground pins ***shall*** be isolated from the module case and chassis ground within the module.
2. ***shall*** be pulled up with 4.7 kΩ to 10 kΩ to a voltage between 3.15 V and 3.45 V on the host board.
3. ***shall*** be pulled up with 4.7 kΩ to 10 kΩ to VCC3.
4. They are DC coupled 100 Ω differential lines which *should* be terminated with 100 Ω (differential) at the user SERDES.
5. These are the differential transmitter inputs. They are AC coupled differential lines with 100 Ω differential termination inside the module.
6. Pins that are not connected (NC) ***shall not*** be grounded in the module.

7.2.1. Pin Definitions

7.2.1.1. GND

GND is an internal ground within the module and is the return for the voltage rails. It is isolated from the module case and chassis ground.

7.2.1.2. TX_DIS

TX_DIS is an input pin. When TX_DIS is asserted *high*, the PXFP-WDM module transmitter output ***shall*** be turned off. The TX_DIS pin ***shall*** be pulled up to +3.3 V in the PXFP-WDM module.

7.2.1.3. VCC5

VCC5 is +5.0 VDC and pin. See section 7.3 for input requirements and pin usage.

7.2.1.4. VCC3_Tx

VCC3_Tx is +3.3 VDC pin, supplying power to the transmitter. See section 7.3 for input requirements and pin usage.

7.2.1.5. VCC3_Rx

VCC3_Rx is +3.3 VDC, supplying power for the receiver. See section 7.3 for input requirements and pin usage.

7.2.1.6. SCL

The SCL (Serial Clock) pin is bidirectional and is used to positively edge clock data into each PXFP-WDM module and negative clock data out of each device. The SCL line *may* be pulled *low* by an PXFP-WDM module during clock stretching.

7.2.1.7. SDA

The SDA (Serial Data) pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven and *may* be wire-ORed with any number of open-drain or open collector devices.

7.2.1.8. MOD_ABS

MOD_ABS is pulled up to Host_Vcc on the host board and grounded in the PXFP-WDM module to indicate that the module is present. Mod_Abs goes *high* when the PXFP-WDM module is physically absent from a host slot.

7.2.1.9. Rx_10G_N

The Rx_10G_N pin is used for the receive inverted 10G data output. It is the negative-side connection in a 100 Ω differential signal pair.

7.2.1.10. Rx_10G_P

The Rx_10G_P pin is used for the receive non-inverted 10G data output. It is the positive-side connection in a 100 Ω differential signal pair.

7.2.1.11. Rx_1G_N

The Rx_1G_N pin is used for the receive inverted 1G data output. It is the negative-side connection in a 100 Ω differential signal pair.

7.2.1.12. Rx_1G_P

The Rx_1G_P pin is used for the receive non-inverted 1G data output. It is the positive-side connection in a 100 Ω differential signal pair.

7.2.1.13. TX_10G_N

The TX_10G_N pin is used for the transmit mode inverted 10G data output. It is the negative-side connection in a 100 Ω differential signal pair.

7.2.1.14. TX_10G_P

The Tx_10G_P pin is used for the transmit mode non-inverted 10G data output. It is the positive-side connection in a 100 Ω differential signal pair.

7.3. DC Power Requirements

The host has three power supplies: two at +3.3 V and one at +5.0 V. The host filters to reduce the noise between each module and the noise between the power supplies. Each pin is limited to 0.5 A.

The host ***shall*** provide power characterized per Table 4 of [XFP MSA], with the following exceptions:

- VCC2 (the 1.8 V pin) is not implemented.
- VEE5 (the -5.2 V pin) is not implemented.
- VCC3 applies to both the VCC3_Tx and VCC3_Rx pins.
- The Maximum Current Inrush ***shall*** be limited to 0.5 A for each VCC3_Tx and VCC3_Rx pins.
- Where specified differently in Table 5.

Table 5 – Power per Rail

Rail	Voltage	Max Current Required	Resulting Power per Rail	Pin
VCC3_Tx	+3.3 V	0.76 A[1]	2.5 W	8
VCC3_Rx				9
VCC5	+5.0 V	0.5 A	2.5 W	6
[1] Combined Tx and Rx current				

The sum of all powers ***shall not*** exceed the limits set by the XFP power class 3, as specified in [XFP MSA].

7.3.1. Host Power Noise Output

To limit wide band noise power, the host system and module ***shall*** each meet a maximum of 2% peak-peak noise when measured with a 1 MHz low pass filter. In addition, the host system and the module ***shall*** each meet a maximum of 3% peak-peak noise when measured with a high pass filter from 1 MHz to 10 MHz. To limit wide band noise power, the host system and module ***shall*** each meet a maximum peak-peak noise, as specified in [XFP MSA].

The PXFP-WDM port on a host board is tested with a resistive load in place of the PXFP-WDM module, each voltage rail at maximum current supported by the host. Voltage is measured at the module side of the PXFP-WDM connector. The test is performed with all other portions of the host board/system active. Hosts with multiple PXFP-WDM modules will test ports one at a time, with active PXFP-WDM modules in all the remaining ports.

The PXFP-WDM module is tested with a high quality power supply connected through the sample filter shown in Figure 3 of [XFP MSA]. Voltage is measured at the host side of the PXFP-WDM connector, between the sample host filter network and the PXFP-WDM module. The PXFP-WDM module ***shall*** pass this test in all operating modes. This test ensures the module will not couple excessive noise from inside the module back onto the host board.

7.3.2. PXFP-WDM Module Power Noise Susceptibility

An PXFP-WDM module ***shall*** meet all electrical requirements and remain fully operational in the presence of noise on all voltage inputs, as detailed in [XFP MSA].

7.4. Low Speed Electrical Specifications

The following section is based on section 2.5 of [XFP MSA] and is presented here with modifications.

Low speed signaling is based on Low Voltage TTL (LVTTL) operating at a nominal supply of (3.3 V ±5%). Hosts ***shall*** use a pull-up resistor connected to a host_Vcc of +3.3 volts (3.15 V to 3.45 V) on the I^2C interface SCL (clock), SDA (Data), and all low speed status outputs.

The PXFP-WDM low speed electrical specifications ***shall*** conform to those listed in Table 6. This specification ensures compatibility between host bus masters and PXFP-WDM SCL/SDA lines and compatibility with I^2C.

Table 6 – Low Speed Control and Sense Signals, Electronic Characteristics

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
TX_Dis	V_{IL}	-0.3	0.8	V	Rpullup pulled to VCC3, measured at PXFP-WDM side of connector. I_{IL}(max) = -10 µA
	V_{IH}	2.0	VCC3_TX +0.3	V	Rpullup pulled to VCC3, measured at PXFP-WDM side of connector. I_{IH}(max) = 10 µA
SCL and SDA	V_{OL}	0.0	0.4	V	Rpullup1 pulled to host_Vcc, measured at host side of connector. I^{OL}(max) = 3 mA
	V_{OH}	host_Vcc3 - 0.5	host_Vcc3 + 0.3	V	Rpullup1 pulled to host_Vcc3, measured at host side of connector.
SCL and SDA	V_{IL}	-0.3	host_Vcc3 *0.3	V	Rpullup1 pulled to host_Vcc3, measured at PXFP-WDM side of connector. I_{IL}(max) = -10 µA
	V_{IH}	host_Vcc3 *0.7	host_Vcc3 + 0.5	V	Rpullup1 pulled to host_Vcc3, measured at PXFP-WDM side of connector. I_{IH}(max) = 10 µA
Leakage Current	I_I	-10	10	µA	
Capacitance for SCL and SDA I/O Pin	C_i		14	pF	10 pF for PXFP-WDM IC I/O pin, 4 pF for PXFP-WDM PCB trace
Total bus capacitive load for SCL and for SDA	C_b		100	pF	At 400 kHz, 3.0 kΩ Rp, max At 100 kHz, 8.0 kΩ Rp, max
			400	pF	At 400 kHz, 0.80 kΩ Rp, max At 100 kHz, 2.0 kΩ Rp, max
1. For combinations of Rpullup (Rp), bus capacitance and speed, see Figures 39 and 44 of [UM10204]. Rise and fall time measurement levels are defined in the XFP management interface ac electrical specifications. Active bus termination *may* be used by the host in place of a pullup resistor, as described in [UM10204].					

7.5. Timing Requirements of Control and Status I/O

The PXFP-WDM module ***shall*** conform to the timing requirements of control and status I/O defined in Table 7.

Table 7 – Timing Parameters for PXFP-WDM Management

Parameter	Symbol	Min	Max	Unit	Conditions
TX_DIS assert time	t_off		10	µs	Rising edge of TX_DIS to fall of output signal below 10% of nominal
TX_DIS negate time	t_on		2	ms	Falling edge of TX_DIS to rise of output signal above 90% of nominal
Time to initialize	t_init		300	ms	From power on or hot plug after supply meeting Table 4 of version 4.5 of [XFP MSA].

The I^2C serial bus timing is described in Chapter 4 of [XFP MSA].

7.6. XFI Signal Conditioner and CDR

The PXFP-WDM module ***shall*** meet the Signal Conditioner requirements specified in section 3.9 of [XFP MSA], with the exception that CDR is only active on transmit. CDR on the receiver ***shall*** be disabled.

8. Mechanical and Board Definition

8.1. Introduction

The mechanical components defined in this section are illustrated in Figure 29 of [XFP MSA]. The module and connector dimensions are constant for all applications, while the bezel, cage assembly, EMI gasket, clip, and heat sink can be designed and/or adjusted for the individual application.

The relatively small form factor of the PXFP-WDM module combined with an adaptable heat sink option allows host system design optimization of module location, heat sink design (shape/dimension/fins), and airflow control. The module can be inserted and removed from the cage with the heat sink and clip attached.

8.2. PXFP-WDM Module Package Dimensions

The PXFP-WDM module package dimensions ***shall*** comply with Section 6.3 and Figures 31 and 32 of [XFP MSA] with the exception of an increase in the overall maximum length of the module, shown in Figure 6.

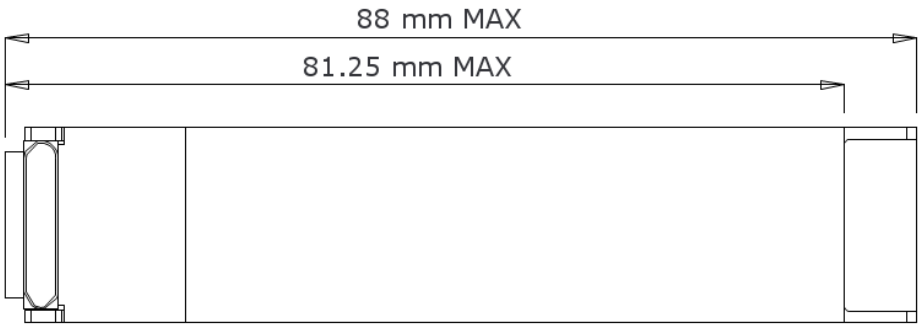

Figure 6 – Length of Module

8.3. Mating of PXFP-WDM PCB Mating Interface to the Host Board Electrical Connector

The PXFP-WDM module PCB electrical interface ***shall*** comply with Section 6.4 and Figure 33 of [XFP MSA]. The length of the contact pads ***shall*** be as defined by the plug sequence in Table 4, where:

- 1 defines a long pad
- 2 defines a medium pad
- 3 defines a short pad

8.4. Host Board Layout

The host board layout to accommodate the PXFP-WDM module ***shall*** comply with Figures 35 and 36 of [XFP MSA].

8.5. Insertion, Extraction and Retention Forces for PXFP-WDM Modules

The PXFP-WDM module insertion, extraction, and retention forces ***shall*** comply with Section 6.6 and Table 61 of [XFP MSA].

8.6. Color Coding and Labeling of PXFP-WDM Modules

The PXFP-WDM module label/marking requirements ***shall*** comply with Section 6.7 of [XFP MSA] and Section 6 of [SFF-8477], except where specified otherwise here.

The PXFP-WDM module ***should*** have a warning label that states the module is not MSA compliant on a yellow label with black text.

The color coding for the wavelength of the PXFP-WDM module ***shall*** be color coded on the latch, bale, or similar locking mechanism, as specified in Table 8.

Table 8 – PXFP-WDM Module Color Coding

Plan	Tx Center Wavelength	Rx Detector Type	Color
DWDM	1550 nm	APD	White with Black Center Stripe
DWDM	1550 nm	non-APD	Red with Black Center Stripe
DWDM	Wavelength-Tunable	APD or non-APD	Green with Black Center Stripe

8.7. EMI Design Using PXFP-WDM Modules

The host bezel and EMI gasket for the PXFP-WDM module ***shall*** be consistent with the recommendations in Section 6.8 and Figures 37 and 38 of [XFP MSA].

8.8. Host Board Electrical Connector Mechanical Specifications

The electrical connector on the host board for the PXFP-WDM module ***shall*** comply with the specifications in Section 6.9 and Figure 39 of [XFP MSA].

8.9. Host Board Cage Assembly Dimensions

The host cage to accommodate the PXFP-WDM module ***shall*** be compatible with the specifications in Section 6.10 and Figures 40 and 41 of [XFP MSA].

8.10. PXFP-WDM Module Cooling

This specification does not define the cooling mechanism of the PXFP-WDM module. The methods and dimensions of those mechanisms are vendor specific.

8.11. Environmental and Thermal

This specification does not define the operational temperature range of the PXFP-WDM module, but it is expected to operate at the manufacturer's specified operational levels from 0 °C to 70 °C case temperature.

The PXFP-WDM module ***shall*** operate at the manufacturer's specified operational levels from 5% to 95% non-condensing relative humidity throughout an altitude range of -60 to 4,000 meters above mean sea level.

The PXFP-WDM module ***shall*** support power level case 3 specified in section G.1 of [XFP MSA].

8.12. Dust/EMI Cover

A Dust/EMI Cover that can be inserted into a cage assembly when no PXFP-WDM module is present ***shall*** be compatible with the specifications defined in Section 6.14 and Figure 44 of [XFP MSA].

8.13. Optical Interface

The optical interface on the PXFP-WDM module ***shall*** be a LC duplex receptacle that meets the requirements specified in [IEC 61754-20].

8.14. Fiber-Optic End-Face Finish and Connector Geometry

The PXFP-WDM module connector end-face finish ***shall*** be UPC. The UPC finish ***shall*** meet the requirements specified in [FINISH]. The UPC geometry ***shall*** meet the UPC requirements specified in [IEC 61755-3-1].

9. Optical Transmitter and Receiver Specifications

9.1. Signal Characteristics

The PXFP-WDM module ***shall*** meet the signal characteristics requirements specified in Table 9. The PXFP-WDM module ***shall*** support DWDM, as defined in [DWDM] and the DWDM grid, as defined in [DWDM-GRID].

Table 9 – PXFP-WDM Signal Characteristics

Parameter	Min	Max	Unit	Notes
Center Wavelength – DWDM	1530.33	1561.42	nm	Ch. 20-59
Spectral Width		1	nm	-20 dB

It is recommended that when DWDM PXFP-WDM modules are used, a paired, even-odd wavelength allocation scheme is employed, where:

- Even channels are assigned to the PXFP-WDM transmitters.
- The adjacent, higher-numbered odd channels are assigned to the corresponding PXFP-WDM receiver.

The channel used for the receiver of the module is thus implied by the transmitter channel – it will always be the transmitter channel + 1. For example, Channels 20 and 21 of a MUX/DEMUX will be connected to a DWDM Ch20 PXFP-WDM module, where Channel 20 is connected to the module's transmitter port and Channel 21 to the module's receiver port.

9.2. Transmitter Characteristics

The PXFP-WDM module ***shall*** meet the transmitter characteristics requirements specified in Table 10.

Table 10 – PXFP-WDM Transmitter Characteristics

Parameter		Min	Max	Unit	Notes
Transmitter Signal Rate		10.31146	10.31354	Gbps	10.3125 nom
High Speed Electrical XFI Interface (Host Transmitter Output)		Compliant to XFI Host Transmitter Output Specifications at B defined in [XFP MSA].			Defined at Point B per [XFP MSA].
Differential Input Impedance		80	120	Ω	
Differential Data Input Swing		120	850	mVp-p	
Data Input Rise/Fall Time		15	40	ps	From 20% – 80% unfiltered[1]
Tx Disable Voltage		2.0	Vcc3+0.3	V	
Tx Enable Voltage		-0.3	0.8	V	
Average Launch Power		0.0	4.0	dBm	
Side Mode Suppression Ratio		30		dB	
Extinction Ratio		8.2		dB	
Optical Output Power	BOL	0.5	4.0	dBm	
	EOL	0.0	4.0	dBm	
Average Power of OFF Tx			-39	dBm	
Transmitter and Dispersion Penalty			2.0	dB	60 km
Relative Intensity Noise $RMA_{15}OMA$			-128	dB/Hz	
Transmitter Reflectance			-10	dB	
Total Jitter			±0.23	UI	
Optical Return Loss Tolerance			15	dB	
1. Assumes the following optical transmit eye mask definition: {x1,x2,x3, y1,y2,y3 }= {0.25, 0.40, 0.45,0.25,0.28, 0.40}					

9.3. Receiver Characteristics

The PXFP-WDM module ***shall*** meet the receiver characteristics requirements specified in Table 11.

Note: Receiver requirements are expected to be met when the transmitter on the extender side of the link is in compliance with the applicable [DWDM] specification.

Table 11 – PXFP-WDM Receiver Characteristics

Parameter	Min	Max	Unit	Notes
Receiver Signal Rate	10.3125 (10G) and 1.25 (1G)		Gbps	
High Speed Electrical XFI Interface (Host Receiver Input)	Compliant to XFI Host Receiver Input Specification at C defined in [XFP MSA].			Defined at Point C in Figure 4, Application Reference Model of [XFP MSA]. Note that only the 10G receiver input is specified in the MSA.
Rx Differential Output Impedance	80	120	Ω	
10 Gbps Rx_Data Differential Output Voltage Amplitude	340	850	mV	
10 Gbps Output High Voltage	VCC3 – 20	VCC3	mV	
10 Gbps Output Low Voltage	VCC3 – 400	VCC3 – 300	mV	
1.25 Gbps Rx_Data Differential Output Voltage Amplitude	340	850	mV	
1G Data Output Differential Swing	400	1600	mVp-p	
10G Data Output Differential Swing	340	850	mVp-p	
1G Data Output Rise/Fall Time			ps	
10G Data Output Rise/Fall Time		45	ps	
1.25 Gbps Output High Voltage	VCC3 – 1085	VCC3 – 880	mV	
1.25 Gbps Output Low Voltage	VCC3 – 1850	VCC3 – 1555	mV	
Rx_LOS High	2.0	VCC3	V	
Rx_LOS Low	0	0.8	V	
Loss of Signal Assert Time		100	µs	
Loss of Signal De-assert Time		100	µs	
1G Receiver Sensitivity (no fiber)		-24	dBm	
1G Receiver Sensitivity (60 km)		-22	dBm	
10G Receiver Sensitivity (no fiber)		-24	dBm	Pre-FEC, BER@10^{-12}, transmitter source has an extinction ratio of 8.2 dB

Parameter	Min	Max	Unit	Notes
10G Receiver Sensitivity (60 km)		-22	dBm	Pre-FEC, BER@10^{-12}, transmitter source has an extinction ratio of 8.2 dB
1G Receiver Optical Overload	-9		dBm	BER@10^{-12}, PRBS 2^7, Receiver Optical Overload P -1, transmitter source has an extinction ratio of 8.2 dB
10G Receiver Optical Overload	-6		dBm	BER@10^{-12}, PRBS 2^{31}, Receiver Optical Overload P -1, transmitter source has an extinction ratio of 8.2 dB
1G/10G Receiver Coexistence Optical Overload	-9		dBm	BER@10^{-12}, 1G PRBS 2^7, 10G PRBS 2^{31}, Receiver Optical Overload P -1, transmitter source has an extinction ratio of 8.2 dB
Damaged Input Optical Power	-5		dBm	
1G Receiver Settling Time		400	ns	
10G Receiver Settling Time		800	ns	
1G Rx_LOS Assert	-45		dBm	
10G Rx_LOS Assert	-42		dBm	
1G Rx_LOS De-assert		-30	dBm	
10G Rx_LOS De-assert		-30	dBm	
Rx_LOS Hysteresis	0.5	5	dB	
Receiver Reflectance		-25	dB	
Consecutive Identical Digit Immunity	72		bits	Per [IEEE 802.3]